REMARKS

Claims 1-7 and 9 are pending in the present application. Claims 1-4 and 9 were rejected. Claims 1, 2, 5, 7 and 9 are herein amended. Claims 8 and 10 are herein cancelled without prejudice.

Applicants' Response to Claim Rejections under 35 U.S.C. §112

Claim 10 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

Claim 10 has been cancelled, and this rejection is now moot.

Applicants' Response to Claim Rejections under 35 U.S.C. § 102

Claims 1-4, 8 and 9 were rejected under 35 U.S.C. § 102(b) as being anticipated by Azuma et al. (JP 2001-274239).

The Examiner argues that **Azuma** discloses all of the limitations claimed in the present application. **Azuma** discloses a semiconductor device with a silicon substrate 1, an interlayer insulation layer 2, a "high dielectric constant film" 4, a "low dielectric constant film" 5, a wiring line 8w and a plug 8p. The interlayer insulation layer 2 is made of SiO_2, the film 4 is made of TEOS, and the film 5 is made of organic SOG or porous silica, for example. Thus, the interlayer

insulation layer 2 and high dielectric constant film 4 both have high dielectric constants. The low dielectric constant film 5 has a low dielectric constant.

The present invention discloses a silicon substrate 1, a planarized via layer insulating film 5, a protective film 6, a via layer insulating film 7, wiring trench 16 and conductive plug 11. The planarized via layer insulating film is made of PSG and has a high dielectric constant, while the via layer insulating film is made of, for example, porous silica, and has a low dielectric constant.

Thus the present application differs from **Azuma** in that it recites a first insulating film formed over the semiconductor substrate and a second insulating film having a lower dielectric constant formed over the first insulating film. **Azuma** instead discloses a first interlayer insulation layer 2, a high dielectric constant film 4, and a low dielectric constant film 5 formed over the high dielectric constant film.

Although the Examiner argues that "[t]hese are all of the limitations set forth in claims 1-4," the Examiner does not explain where **Azuma** teaches "a semiconductor element formed over a surface of a semiconductor substrate" and "the first insulating film covering the semiconductor element." Since the Examiner refers to insulating film 4 as the first insulating film, it is presumed that the Examiner considers the metal wiring 3 as the semiconductor element.

With regard to claim 1, Applicants amend the claim to specify "a semiconductor element formed directly on a surface of a semiconductor substrate" and "a first insulating film formed directly on the surface of the semiconductor substrate." Furthermore, Applicants similarly amend the recitation of claim 9, which are directed at a method of manufacturing.

As amended, **Azuma** does not read on claim 1 or claim 9 of the present invention. **Azuma** essentially discloses two insulating layers having a high dielectric constant. Thus, high dielectric constant film 4 of **Azuma** may not be compared to planarized via layer insulating film 5 of the present invention since it is not directly formed on the semiconductor substrate. Entry of the amendments and favorable reconsideration is respectfully requested.

With regard to claim 2, the wiring 8w shown in Figure 4(g) of **Azuma** appears to correspond to the first wiring pattern 19 recited in claim 2. This is because it is formed over the second insulation layer 5_1. In Figure 4(g), metal wiring 3 is disposed below the wiring 8w. Thus, the wiring 8w is not the lower metal wiring among multilevel wirings. In contrast, claim 2 recites that the first wiring pattern 19 is disposed at the lowest level among the wiring patterns made of metal.

Applicants further argue that metal wiring 3 of **Azuma** may not be compared to the first wiring pattern 19. In Figure 4(g) of **Azuma**, the interlayer insulating film 2 in which metal wiring 3 is buried does not have a two-layer structure consisting of a higher dielectric constant film and a lower dielectric constant film as required by claim 2. Therefore, Applicants argue that **Azuma** does not contain an element comparable to the first wiring pattern of the present application. For at least these reasons, Applicants respectfully submit that claim 2, and all claims dependent thereon, distinguish over the cited art. Applicants also note that claim 8 has been cancelled and thus the rejection of claim 8 is moot. Favorable reconsideration is respectfully requested.

Claims 1-4 and 8-10 are rejected under 35 U.S.C. § 102(e) as being anticipated by Tanaka et al. (U.S. Patent No. 6,838,771)

The Examiner argues that **Tanaka** discloses all of the limitations recited in claims 1-4 and 8. Applicants note that claims 8 and 10 have been cancelled and thus rejections of those claims are moot. **Tanaka** discloses a semiconductor device where a substrate 601 has a semiconductor element 602 and 603 formed on it. These are covered by SiO film 604, BPSG film 605, silicon carbonitride film 607. The Examiner points to BPSG film 605 as the first insulating film, however, the SiO film also functions as an insulator. See column 14, line 65 to column 15, line 6. As the claims now recite that the first insulating film is directly on the semiconductor substrate and element, the SiO film 604 must be comparable to the first insulating film.

On the other hand, the present application recites a semiconductor element directly on a semiconductor substrate and a first insulating film directly on the semiconductor substrate and element. The claims also recite "a top surface of the first insulating film being planarized." As shown in Figure 1 of the present application, the top surface of planarized via layer insulating film 5 is flat. In contrast, according to Figure 6 of **Tanaka**, the SiO film 604 is not planarized, but rather is formed in an irregular manner.

With regard to claim 9, which recites a method of manufacturing, **Tanaka** does not disclose the planarization of the first insulating film formed directly on the semiconductor

substrate and element. For at least these reasons, Applicants respectfully submit that the claims distinguish over the cited art. Favorable reconsideration is respectfully requested.

Allowable Subject Matter

The Examiner objected to claims 5-7 as being dependent on a rejected base claim, but notes that these claims would be allowable if re-written in independent form. Applicants herein amend claims 5 and 7 to be in independent form. Claim 6 remains dependent on claim 2.

For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned agent.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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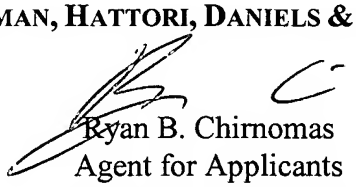

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